(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 883 325 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
09.12.1998 Bulletin 1998/50

(51) Int Cl.[6]: **H04R 3/00**

(21) Application number: **98304349.8**

(22) Date of filing: **02.06.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **02.06.1997 AU PO7141/97**

(71) Applicant: **THE UNIVERSITY OF MELBOURNE**
Parkville, Victoria 3052 (AU)

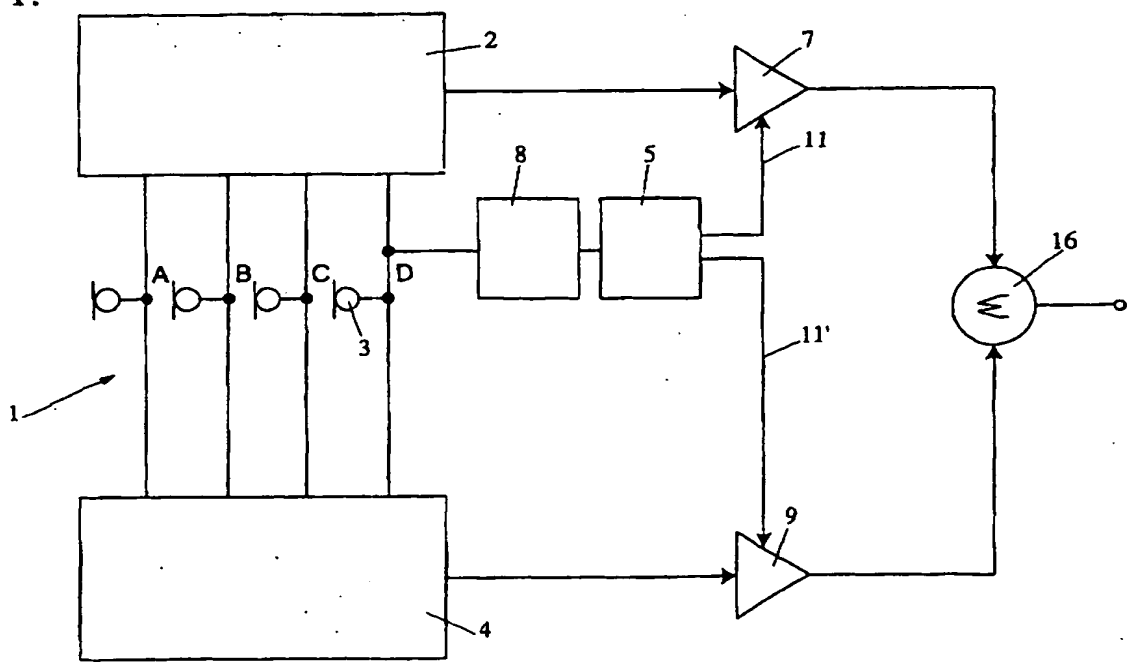
(72) Inventors:
- **Raicevich, George**
  Stanmore, N.S.W. 2204 (AU)
- **Dillon, Harvey**
  Turramurra, N.S.W. 2074 (AU)

(74) Representative: **Molyneaux, Martyn William**
Langner Parry
52-54 High Holborn
London WC1V 6RR (GB)

(54) Multi-strategy array processor

(57) An apparatus and method for processing sound, suitable for use in association with a hearing aid, cochlear implant prosthesis or the like. Coupled to an array of microphones (1) are a pair of fixed array processors (2,4) each having different characteristic signal-to-noise performances and internal noise parameters in different levels of ambient noise. Based upon an ambient noise estimate derived from noise floor detector (8) a control circuit (5) controls the gain of a pair of VCA's (7,9) coupled to the fixed array processors (2,4) in order to produce an output signal from summer (16) which maximises the signal-tonoise ratio of a signal emanating from a source in an on-beam direction relative to the microphone array (10).

Fig 1.



EP 0 883 325 A2

Description

FIELD OF THE INVENTION

The present invention relates to the field of devices for improving the speech perception of hearing impaired subjects. Such devices include acoustic hearing aids, tactile aids, cochlear prostheses and brain stem implants. In particular the invention is concerned with optimising the intelligibility of speech delivered to a subject by means of a directionally discriminating device.

BACKGROUND

In general the effects of hearing impairment are characterised by the undesirable conditioning of a speech signal along the subject's hearing chain so as to result in attenuation and often distortion of the signal. It has been found that a standard hearing aid which amplifies the ambient sound can compensate for hearing losses attributable to attenuation, however such systems are of little assistance in low signal-to-noise ratio conditions.

Therefore, while most hearing aids provide substantial relief to the hearing impaired in single speaker, low reverberation, environments they are less useful where several speech sources are present simultaneously with the one of interest to the subject or when used in a room exhibiting strong reverberation characteristics. This poor performance is because such conditions are more likely to result in a lower speech signal-to-noise ratio than is prevalent in a single speaker, low reverberation environment. The problem of aiding a hearing impaired subject in a noisy environment is not overcome merely by indiscriminately amplifying both the speech of interest as well as the background noise.

In order to address this problem directional hearing aids have been used. Such hearing aids are able to spatially discriminate between sound sources. These aids selectively amplify sound sources in a particular direction or "beam" relative to the aid.

A common method for producing spatial discrimination in a sound field has been to process the outputs from an array of microphones. Both fixed and adaptive array processors have been used. The principal property of adaptive array processors is that the microphone weights are continually adjusted with the array being statistically optimised according to some criterion. A problem with the adaptive array is that in a reverberant environment the processor may be unable to determine the direction of the desired signal and hence the weights to be adjusted. Consequently adaptive array processors will not be discussed further. In contrast, in a fixed array processor the signal processing components of the array are time-invariant, the fixed array using data independent weights and delays applied to the microphone outputs to create a maximum sensitivity to signals coming from a desired direction. There are many different types and configurations of fixed array processors. Each such processor has associated with it a degree of directivity and a particular level of inherent noise.

For example, one fixed processing arrangement which is well known in the art is based on addition and appropriate delay of the separate microphone outputs. Such an additive processor exhibits only moderate directionality however it can be used in relatively quiet environments because it has a greater signal-to-noise ratio than many more directional types of processor or indeed even a single microphone.

An alternative method for achieving spatial discrimination is to subtract the output of some of the separate microphones from the others. In this case the level of subtraction involved determines the amount by which off-beam sounds are suppressed. For example, second order subtraction, by which difference signals are subtracted from each other, affords a greater degree of suppression than first order subtraction, by which difference signals are added to each other, but has the disadvantage that whilst it strongly attenuates off-beam sounds it also attenuates the wanted signal to such an extent that internal microphone noise becomes significant when used in quiet surroundings. While subtractive processing has a higher directional performance than additive processing its ratio of signal to internal noise is poorer than that of the additive processor because of the increased on-beam attenuation. Details of the construction and theory of additive and subtractive sound processors are described in *Speech Intelligibility Enhancement Technique : Multi Microphone Array* by G. Raicevich - a Thesis for the degree of Master of Engineering, available from the library of the University of Technology Sydney, Broadway, Sydney, Australia.

In general, fixed array processors which have a relatively high directional performance and a relatively lower ratio of signal to internal noise, in quiet environments, such as the above described subtractive processor, are more suited to use in high noise situations. However in lower noise environments the converse is true and so it is preferable to use a fixed array which, whilst it may exhibit a lower directionality has the advantage of a significantly higher ratio of signal to internal noise.

Another type of fixed array processor is the so-called "Supergain". The constrained supergain array described in the paper *Practical Supergain,* by Henry Cox et al (IEEE Transactions on Acoustics Speech and Signal Processing Vol ASSP- 34 No. 3 June 1986), applies complex weights to the individual microphone outputs of a microphone array. By modifying a frontal gain constraint the values of the weights may be calculated and the qualities of the supergain array may be controlled. For example, a supergain array processor may incorporate weighting which takes the background noise characteristics into account. In high background noise the resulting processor will have a lower frontal gain constraint and hence a higher directivity. The associated higher array internal noise will not unduly affect the sig-

BNSDOCID: <EP 0883325A2 I >

nal-to-noise ratio. Conversely, when designing a supergain processor for use in a low background noise level environment, a higher frontal gain constraint will result in a lower directivity but a lower array internal noise.

While a fixed array processor may operate well in a particular noise environment its characteristics may not be ideal for operation as the background noise level of its environment changes. Consequently there is a need for a hearing aid which, while compact is also directional and able to adjust to changes in the noise environment without the drawbacks associated with adaptive arrays.

It is an object of the present invention to provide a system by which a fixed array processing strategy is determined according to prevailing environmental conditions. preferably the level of ambient noise floor, so as to maximise the speech signal-to-noise ratio of a spatially discriminating aid for the hearing impaired.

It is a further object of the present invention to provide a system by which the complex weights of a constrained supergain array may be adjusted in order to maximise the overall signal-to-noise ratio of the processor given the prevailing acoustic environment in which the array is used.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention there is provided a method for processing sound comprising the steps of :

a) determining the signal-to-noise performance of a plurality of fixed microphone array processors for a range of ambient noise levels;
b) monitoring a parameter indicative of ambient noise conditions to determine the prevailing ambient noise level;
c) determining the operating parameters of a microphone array processor being the microphone array processor of said plurality of microphone array proccessors having the highest signal-to-noise performance in the prevailing ambient noise level; and
d) processing the output of a microphone array with a processor having the operating parameters of the processor selected in step c).

According to a further aspect of the present invention there is provided An apparatus for processing sound comprising :

a) an array of microphones;
b) first and second array processors coupled to said array, each of said processors arranged to produce a characteristic total noise output being a function of ambient noise floor,
the first processor being arranged to produce a lower characteristic total noise output than the second processor over a first range of values of noise floor, and the second processor being arranged to produce a lower characteristic total noise output than the first processor over a second range of values of said noise floor;
c) a noise floor indicating circuit coupled to at least one microphone of said array of microphones arranged to produce a noise floor signal indicative of said ambient noise floor;
d) control means coupled to said noise floor indicating circuit and arranged to produce first and second control signals indicating when said noise floor signal is in said first range of values or in said second range of values;
e) first and second variable gain means,
the first and second variable gain means being coupled to the first and second microphone array processor, and being responsive to the first and second control signal respectively,
the first and second variable gain means arranged to apply variable gain to the characteristic total noise output of the first and second array processor, respectively,
the control means and said first and second variable gain means being further arranged so that the gain applied by the first variable gain means is greater than the gain applied by the second variable gain means when said noise floor signal is within said first range and the gain applied by the second variable gain means is greater than the gain applied by the first variable gain means when said noise floor is within said second range.

According to a further aspect of the invention there is provided an apparatus for processing sound comprising :

a) an array of microphones;
b) first and second array processors coupled to said array of microphones, each of said processors arranged to produce a characteristic total noise output being a function of ambient noise,
the first processor being arranged to produce a lower characteristic total noise output than the second processor over a first range of values of ambient noise, and the second processor being arranged to produce a lower characteristic total noise output than the first processor over a second range of values of said ambient noise;
c) background noise processor coupled to said microphone array and arranged to have maximum sensitivity to background noise said background noise processor producing a background noise signal;
d) on-beam signal detect circuit responsive to said background noise processor and to output from said first and second array processors for producing a detect signal indicative of the presence of on-beam signal;
e) first and second sample-and-hold circuits cou-

pled to said first and second processors respectively and being responsive to said detect signal, said first and second sample-and-hold circuits arranged to produce first and second ambient noise estimates;

f) control circuit coupled to said first and second sample-and-hold circuits and arranged to produce first and second control signals to indicate relative magnitudes of said first and second noise estimates;

g) first and second variable gain circuits coupled to the first and second array processor, respectively,

the first and second variable gain circuits being responsive to the first and second control signal, respectively,

and arranged to apply variable gain to the characteristic total noise output of the first and second array processor, respectively,

the control circuit and said first and second variable gain circuits being further arranged so that when said first noise estimate is less than said second noise estimate said gain applied by the first variable gain circuit is greater than said gain applied by the second variable gain circuit and when said second noise estimate is less than said first noise estimate said gain applied by the second variable gain circuit is greater than said gain applied by the first variable gain circuit.

According to a final aspect there is provided an apparatus for processing sound comprising :

a) a microphone array comprising a plurality of microphones each microphone producing a signal corresponding to surrounding ambient sound;

b) a plurality of antialiasing filters coupled to each microphone of said array respectively, each antialiasing filter arranged to produce a low-pass filtered signal;

c) a plurality of analog to digital converters coupled to each antialiasing filter respectively, each analog to digital converter arranged to produce a digital noise signal ;

d) a microphone array processor coupled to said analog to digital converters arranged to produce a noise level signal indicative of the ambient noise level;

e) an allocation means responsive to said noise level signal and arranged to produce a plurality of weighting signals in accordance with a predetermined rule;

f) a plurality of digital multiplier means coupled to each analog to digital converter and respectively responsive to said plurality of weighting signals, each said multiplier arranged to perform a complex multiplication operation on each digital noise signal respectively, said plurality of digital multipliers producing a corresponding plurality of multiplied signals;

g) means for delivering said plurality of multiplied signals for further processing.

The invention also extends to acoustic hearing aids, tactile aids, cochlear prostheses, brain stem implants and other aids to hearing which incorporate the above described inventive features.

DESCRIPTION OF THE DRAWINGS

Figure 1 depicts the present invention according to a first embodiment.

Figure 2 depicts the relative performance in varying background noise of two different microphone array processors.

Figure 3 depicts three regions of the graph shown in Figure 2.

Figure 4 depicts the present invention according to a second embodiment.

Figure 5 depicts the present invention according to a third embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described according to a preferred embodiment. Referring now to Figure 1, depicted is a microphone array 1 consisting of a number of microphones. In the present example four microphones are shown however other numbers are also possible and the invention is not limited to the number of microphones used herein. The outputs of the microphones are labelled from A to D. According to a first embodiment the microphone outputs are passed to two different signal processing modules named Yss and Ysa and denoted as items 2 and 4 respectively.

Although in the present example only two processors are shown it is possible to have a greater number of processors in which case selection between them is also made according to the criteria explained herein. Furthermore the invention may be embodied by means of a single processor configurable into two or more modes. In that case selection between processing modes is also made according to the criteria explained herein.

Returning now to the embodiment of Figure 1, relative to Ysa the first signal processing module Yss 2 is characterised by having a greater directionality but also a lower ratio of signal to internal noise. In contrast the second signal processing module Ysa has a higher ratio of signal to internal noise and a lower degree of directionality.

One of the microphones 3 of the array is monitored and its output passed to a noise floor indicating circuit 8. Such circuits are known in the art, for example, a simple noise floor indicating circuit typically consists of an AC coupling capacitor followed by a rectifier and low pass filter. As the noise floor usually has a magnitude

similar to the signal envelope, monitoring of the envelope provides an indication of the noise floor subsequent to appropriate scaling.

The output of the noise floor detector comprises a relatively slowly moving DC signal indicative of the ambient noise floor. The DC signal from the noise floor indicator is coupled to control circuit 5. Emanating from control circuit 5 are two control lines 11 and 11'. Control circuit 5 contains an inverting amplifier which is connected between the output from the noise floor detector 8 and control line 11'. It also contains a buffer amplifier or depending on the remainder of the circuitry used a conductor, connected between the output of the noise floor detector 8 and control line 11. Control line 11' is connected to voltage controlled amplifier 9 which is also connected to the output of Ysa, 4. Contol line 11 is similarly connected to voltage controlled amplifier 7 which is also connected to the output of Yss, 2.

The outputs of VCA 7 and VCA 9 are added together by summer 16, which may consist of an appropriately configured operational amplifier, and then passed to a conventional hearing aid device (not shown).

Referring now to Figure 2 the operation of the device will be explained. Figure 2 illustrates the noise discrimination ability for the subtractive 2 and additive 4 processors. The Figure depicts the characteristic outputs of Ysa and Yss in dB's on the vertical axis plotted againsT ambient acoustic noise floor, in dBs on the horizontal axis. It will be noted that as the ambient noise falls to low values, depicted as region A of Figure 3, the. output of Yss 2 and Ysa 4 are substantially due to electrical noise internally generated in the processors and microphone array. A lower processor output for a given noise floor level indicates a higher directivity and hence better sound discrimination ability. It is seen from the graph of Figure 2 that the Yss processor output, line 17 indicates a better performance when the noise floor has a high value, i.e. to the right of the intersection point of the two curves. Whereas the Ysa output, line 18 is lower in low acoustic ambient noise conditions. The graph also shows that both array outputs plateau in the lower noise regions. As the ambient noise levels drop, the array outputs remain constant. Such plateauing indicates that the array output is dominated by internally generated noise. The subtractive processor Yss, while exhibiting greater spatial discrimination, also produces more internal noise as is evident by the relatively high plateau, line 22, found on the left hand side of its plot, relative to the plateau of Ysa, depicted by line 20.

According to the invention the noise floor detector 8, control circuit 5 and VCA's 7, 9 are scaled so that as the noise floor indicative signal drops VCA 7 attenuates whilst the gain of VCA 9 increases so that the output of summer 16 is substantially Ysa, which is appropriate for the low noise environment. Alternatively, as the ambient noise increases the second order subtractive processor Yss becomes preferred and so by the design of the device in Figure 1 VCA 7 increases its gain whilst that of VCA 9 is attenuated, the output of summer 16 becoming substantially that of Yss.

Referring now to Figure 3 there is depicted a version of Figure 2 wherein the acoustic ambient noise has been demarcated into three ranges A, B and C. It can be seen that VCA's 7 and 9 are controlled by the noise floor detector 8 so that the output of the summer 16 predominantly consists of the output of the processor which provides the lowest total noise output. Consequently, in region A of the graph the output of the summer consists entirely of signal from Ysa 4. In region B of the graph the output of the summer consists of a mixture of both processors. Leftward of the point at which the curves 17, 18 characteristic of each of the processors intersect the summer output is increasingly Ysa 4. Rightward of the intersection point it is increasingly Yss 2. At the point of intersection it is equally due to signal from Ysa and Yss. In region C of the graph the output of the summer consists entirely of signal from Yss.

In practice the system is calibrated for switchover by noting the output from the noise floor detector at which the intersection of curves 17 and 18 occurs. The VCA's are then adjusted so that complete switchover from one processor to the other takes place within a cross-over range centred on the intersection point. It has been found that a cross-over range a little greater than 6dB is required in order to minimise the subject's perception of the change in processing strategies. Whilst the blending of the two signals which occurs in cross-over range B is not essential to the invention, it makes the device more comfortable for the subject by reducing the perception of the switching between processing strategies. Consequently the invention could be implemented by automatically switching between the two strategies at the point where their characteristic processor curves intersect rather than blending the output of the two processors across cross-over range B. Furthermore, although not incorporated into the embodiments herein described, hysteresis could be introduced into the switching or blending operation so that switch over would occur at different values of external noise depending on whether the external noise was increasing or decreasing.

According to a further embodiment of the present invention an auto switching arrangement comprising processor microphone array processor Yn, signal detector circuit 40 and sample-and-hold (S/H) circuits 41 and 42 is provided. The S/H circuits contain magnitude estimator circuits, to receive signal from Ysa 4 and Yss 2, comprising a rectifier and low pass filter to generate a rectified and time averaged value indicative of the magnitude of the signal emanating from Ysa and Yss. The S/H circuits are under command of on-beam signal detector 43 from which they take a control signal which determines whether they are to sample signal derived from Ysa and Yss, or to hold. The auto switch-over system automatically chooses the most appropriate proportions of output of array processors Yss 2 and Ysa 4 in

order to maximise the ratio of desired signal to undesired ambient noise. The ambient noise output by the processors is a combination of acoustic ambient noise and electrical noise emanating from the processors and microphone array.

On-beam signal detector 40 takes two inputs. A first input emanates from processor Yn 43. Processor 43 is a microphone array processor whose output is minimally sensitive to the on-beam signal that processors Ysa and Yss are designed to maximise. For example if the device of Figure 4 were to be used in a crowded room, including people speaking and other sound sources, then whilst Ysa and Yss are designed to optimise the signal coming from a particular direction relative to the microphone array, and minimise the remaining noise, Yn, in contrast generates an output that monitors the remaining noise. The inventors have found that a processor constructed similarly to Ysa or Yss except having maximum sensitivity in a direction opposite to the desired on-beam direction of Yss and Ysa, is suitable for this purpose.

The second input to signal detector 40 emanates from the output of summer 16 which is a combination of signals from Yss 2 and Ysa 4.

Signal detector 40 takes the signal from Yn 43 and produces an estimate of its average value over a short period of time, this may be done by rectifying the signal and then low pass filtering it as was described in respect of noise floor indicating circuit 8 of Figure 1. Signal detector 40 also processes the signal from summer 16 in a similar manner. The two rectified and averaged signals are then compared to produce their difference being the processed signal from Yn 43 minus the processed signal from summer 16. The difference signal is passed through a comparator. The comparator produces a logic high detect signal in the event that the difference signal is positive and a logic low detect signal in the event that it is less than or equal to zero. Accordingly, if the signal coming from the summer is of greater magnitude than the signal from processor Yn 43 then signal detector 40 will generate a logic low signal which will indicate that the output of summer 16 contains signal other than ambient noise. Conversely, if the signal coming from processor Yn 43 is of greater magnitude than the signal from summer 16 then signal detector 43 will generate a logic high output to indicate that the output of summer 16 does not contain signal of interest.

In the event that the output of summer 16 does contain signal of interest the detect signal will be low. In that case S/H circuits 41 and 42 hold their current values so that the output of differential amplifier 39 remains constant. In that event the gains of VCA's 7 and 9 remain constant so that there is no change in the relevant propotions of the signals from Ysa 4 and Yss 2 delivered to summer 16.

Alternatively, in the event that the output of summer 16 does not contain signal of interest, the detect signal will be high. In that case S/H circuit 41 will track signal from Yss 2 while signal from Ysa 4 will be tracked by S/H circuit 42. During this state the outputs of S/H circuits 41 and 42 will be approximately the same as those from processors Yss 2 and Ysa 4. Accordingly, when the ambient noise level is low, i.e. the processors are operating in region A of Figure 3, then the output of S/H circuit 41 will be greater than the output of S/H circuit 42. Consequently, the output of differential amplifier 39 will be negative so that the gain of VCA 7 will be low relative to the gain of VCA 9. It should be noted that the control signal for VCA 9 is passed through inverter 10 so that it is of opposite polarity to that which controls VCA 7. As a result the output of summer 16 will be predominantly signal from Ysa 4 which, as can be seen from Figure 3, is of markedly lower noise in Region A than that of Yss 4.

When the ambient noise level is within Range B of Figure 3 then the gain applied to VCA's 7 and 9 will be largely equal so that output from both Yss 2 and Ysa 4 with the output of summer 16 comprised of approximately 50% signal from each of those processors.

Finally when the ambient noise climbs into Region C of the graph the output of Ysa 4 will be greater than that of Yss 2 so that the output of differential amplifier 39 will be positive. Accordingly more gain will be applied to output from Yss 2 than from Ysa 4 and the output of summer 16 will be predominantly due to signal from Yss 2, which has a lower noise level in the Region C range of operation.

Referring now to Figure 5 there is depicted an embodiment of the present invention as applied to a constrained supergain array processor. Such a processor conventionally consists of a series of microphones 51-54 spaced less than one half wavelength, of the centre frequency of the band to be processed, apart. The outputs of each microphone are each multiplied by a complex weight z1..z4, by complex multipliers 61-64. This operation is most conveniently performed using digital techniques and so, prior to multiplication, the signals are passed through anti-aliasing filters 71-74 and converted to digital signals by ADC's 81-84 according to standard methods.

It is known to calculate the weights z1..z4 for a single level of ambient acoustic noise. However, such an approach does not provide for changes in the background noise level which may render the processor less than effective as noise levels change. According to the invention, as background noise levels increase the weights may be altered so that the directionality of the processor may be increased without introducing unwanted instabilities into the processor. Conversely, as the background noise level decreases it is necessary to reduce the directionality of the processor in order to minimise the total noise at the output of the summer 66.

According to the present invention noise level processor Yn 56 and allocation means, being look up table 58, are provided to alter the weights z1..z4. Processor Yn generates an estimate of the ambient acoustic noise level. This estimate is sent to look up table 58 which

contains a list of precalculated values for z1..z4 for given values of ambient acoustic noise level. Calculation of the weighting values is described in the formerly referenced paper by Cox et al.

As a variation to the use of a look up table it is possible to instead calculate the values for the weights as required. In that case the allocation means would not consist of look-up table 58 but instead would be replaced by calculations undertaken in a central digital signal processor or alternatively by a suitable co-processor.

The weighted digital signals are combined, shown schematically by summer 66, and the resulting signal optionally converted to an analog signal by DAC and associated anti-imaging filtering 68.

Although the invention has been described with reference to a limited number of embodiments other variations are possible within the inventive concept and will be apparent to those skilled in the art.

Claims

1. An apparatus for processing sound comprising :

a) an array of microphones;
b) first and second array processors coupled to said array, each of said processors arranged to produce a characteristic total noise output being a function of ambient noise,
the first processor being arranged to produce a lower characteristic total noise output than the second processor over a first range of values of said noise, and the second processor being arranged to produce a lower characteristic total noise output than the first processor over a second range of values of said said noise;
c) a noise floor indicating circuit coupled to at least one microphone of said array of microphones arranged to produce a noise floor signal indicative of said ambient ambient noise;
d) control means coupled to said noise floor indicating circuit and arranged to produce first and second control signals indicating when said ambient noise signal is in said first range of values or in said second range of values;
e) first and second variable gain means,
the first and second variable gain means being coupled to the first and second microphone array processor, and being responsive to the first and second control signal respectively,
the first and second variable gain means arranged to apply variable gain to the characteristic total noise output of the first and second array processor, respectively,
the control means and said first and second variable gain means being further arranged so that the gain applied by the first variable gain means is greater than the gain applied by the second variable gain means when said ambient noise signal is within said first range and the gain applied by the second variable gain means is greater than the gain applied by the first variable gain means when said ambient noise is within said second range.

2. An apparatus according to claim 1, further comprising a summing means coupled to said first variable gain means and to said second variable gain means.

3. An apparatus according to claim 1, wherein the first array processor is a subtractive processor.

4. An apparatus according to claim 1 or claim 3, wherein the second array processor is an additive processor.

5. An apparatus according to claim 1, wherein the control means and first and second variable gain means are further arranged so that the gain applied by the first variable gain means gradually increases and the gain applied by the second variable gain means gradually decreases as said ambient noise signal takes values across a sub-range from a starting value within said second range to a terminating value within said first range.

6. An apparatus according to claim 1, wherein the control means and first and second variable gain means are further arranged so that the gain applied by the first variable gain means gradually decreases and the gain applied by the second variable gain means gradually increases as said ambient noise signal takes values across a sub-range from a starting value within said first range to a terminating value within said second range.

7. An apparatus according to claim 5 or claim 6, wherein the control means and the first and second variable gain means are further arranged so that said sub-range is centred at the value of ambient noise signal where said first and second ranges are in contiguity.

9. An apparatus according to claim 1, wherein the first and second variable gain means comprise voltage controlled amplifiers, and wherein said first and second control signals are voltage signals.

10. An apparatus for processing sound comprising :

a) an array of microphones;
b) first and second array processors coupled to

said array of microphones, each of said processors arranged to produce a characteristic total noise output being a function of ambient noise,

the first processor being arranged to produce a lower characteristic total noise output than the second processor over a first range of values of ambient noise, and the second processor being arranged to produce a lower characteristic total noise output than the first processor over a second range of values of said ambient noise;

c) background noise processor coupled to said microphone array and arranged to have maximum sensitivity to background noise said background noise processor producing a background noise signal;

d) on-beam signal detect circuit responsive to said background noise processor and to output from said first and second array processors for producing a detect signal indicative of the presence of on-beam signal;

e) first and second sample-and-hold circuits coupled to said first and second processors respectively and being responsive to said detect signal, said first and second sample-and-hold circuits arranged to produce first and second ambient noise estimates;

f) control circuit coupled to said first and second sample-and-hold circuits and arranged to produce first and second control signals to indicate relative magnitudes of said first and second noise estimates;

g) first and second variable gain circuits coupled to the first and second array processor, respectively,

the first and second variable gain circuits being responsive to the first and second control signal, respectively,

and arranged to apply variable gain to the characteristic total noise output of the first and second array processor, respectively,

the control circuit and said first and second variable gain circuits being further arranged so that when said first noise estimate is less than said second noise estimate said gain applied by the first variable gain circuit is greater than said gain applied by the second variable gain circuit and when said second noise estimate is less than said first noise estimate said gain applied by the second variable gain circuit is greater than said gain applied by the first variable gain circuit.

11. An apparatus according to claim 10, further comprising a summing means coupled to said first and second variable gain circuit to produce a summation output signal.

12. A method for processing ambient sound comprising the steps of :

a) monitoring said sound by means of an additive array processor and a subtractive array processor, said processors being coupled to a common microphone array and producing processed signals;

b) determining which of said processed signals has the greatest signal to noise ratio for a given ambient noise;

c) selecting the processed signal determined in step b) for further processing.

13. A method according to claim 12, further comprising the step of :

d) summing the processed signals in a ratio wherein a greater proportion of the signal selected in step c) is added.

14. An apparatus for processing sound comprising :

a) a microphone array comprising a plurality of microphones each microphone producing a signal corresponding to surrounding ambient sound;

b) a plurality of antialiasing filters coupled to each microphone of said array respectively, each antialiasing filter arranged to produce a low-pass filtered signal;

c) a plurality of analog to digital converters coupled to each antialiasing filter respectively, each analog to digital converter arranged to produce a digital noise signal ;

d) a microphone array processor coupled to said analog to digital converters arranged to produce a noise level signal indicative of the ambient noise level;

e) an allocation means responsive to said noise level signal and arranged to produce a plurality of weighting signals in accordance with a predetermined rule;

f) a plurality of digital multiplier means coupled to each analog to digital converter and respectively responsive to said plurality of weighting signals, each said multiplier arranged to perform a complex multiplication operation on each digital noise signal respectively, said plurality of digital multipliers producing a corresponding plurality of multiplied signals;

g) means for delivering said plurality of multiplied signals for further processing.

15. An apparatus according to claim 14, wherein the means for delivering output signals comprises a digital summing means responsive to said plurality of multiplied signals.

16. An apparatus according to claim 14, wherein the allocation means comprises a look-up table.

17. An apparatus according to claim 14, wherein the allocation means comprises a computational processor programmed according to said rule.

18. An apparatus according to claim 14 or claim 17, wherein the allocation means allocates weights so that the directionality of the processor increases as said noise level signal increases.

19. A method for processing sound comprising the steps of :

a) determining the signal-to-noise performance of a plurality of fixed microphone array processors for a range of ambient noise levels;
b) monitoring a parameter indicative of ambient noise conditions to determine the prevailing ambient noise level;
c) determining the operating parameters of a microphone array processor being the microphone array processor of said plurality of microphone array proccessors having the highest signal-to-noise performance in the prevailing ambient noise level; and
d) processing the output of a microphone array with a processor having the operating parameters of the processor selected in step c).

20. A method according to claim 19, wherein step b) includes the step of monitoring a microphone of said microphone array.

21. A method according to claim 19, wherein step b) includes the step of monitoring the output of a microphone array processor coupled to said microphone array.

22. A method according to claim 19, wherein step c) includes the step of obtaining said operating parameters from a look-up table on the basis of the prevailing ambient noise level.

23. A method according to claim 19, wherein step c) includes the steps of : passing said prevailing ambient noise level through a control circuit to generate a number of control signals; and monitoring a processor having said operating parameters on the basis of said control signals.

24. A method according to claim 19, wherein step c) includes the step of calculating said operating parameters as a function of the prevailing ambient noise level.

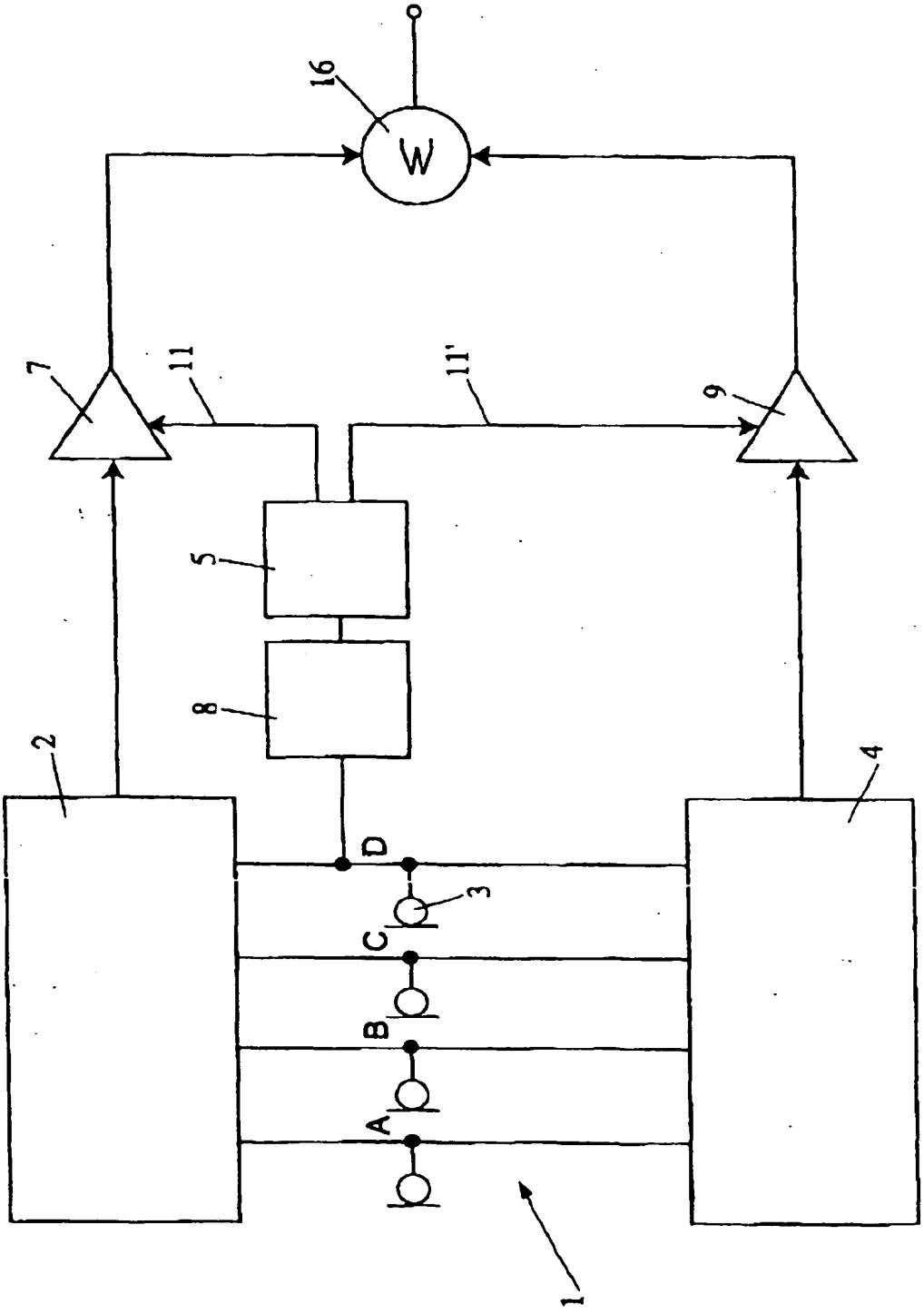


Fig 1.

EPNSDOCID: <EP 0883325A2 | >

Fig 2.

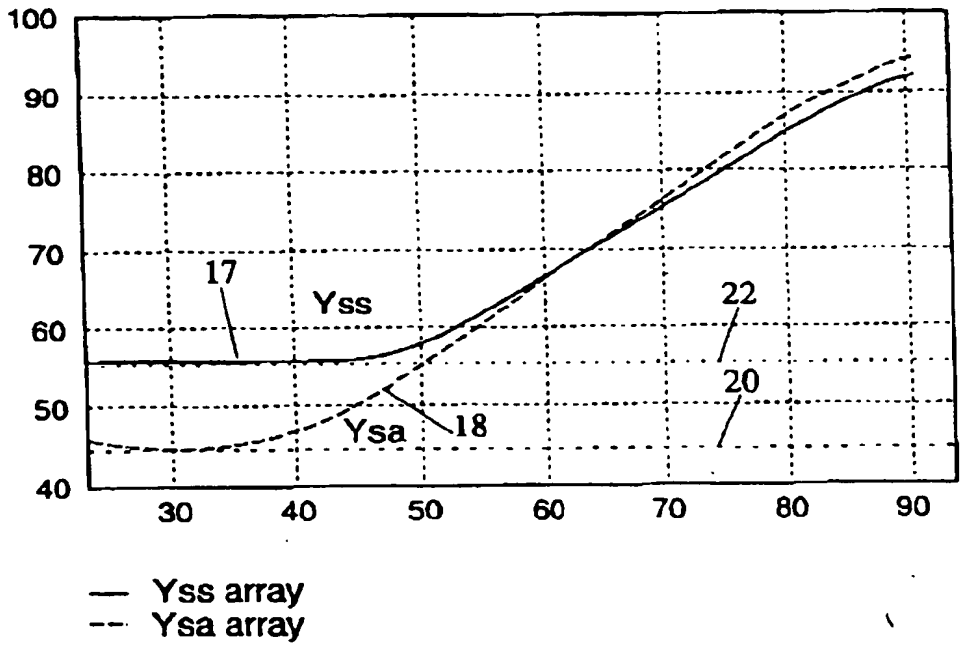
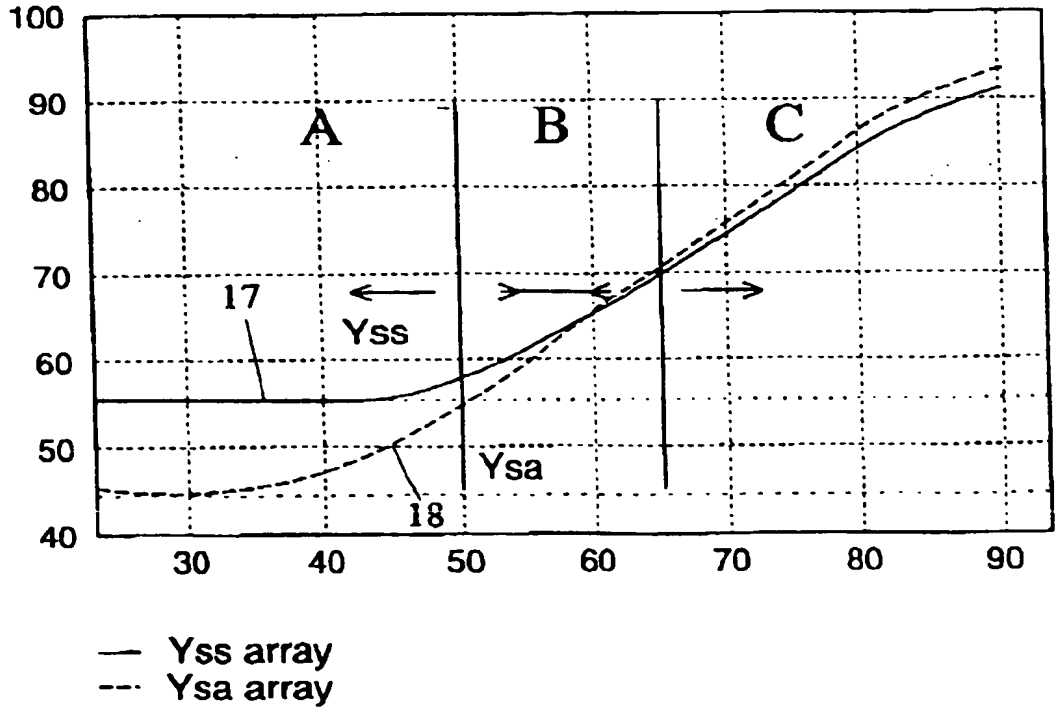

100
90
80
70
60
50
40
30
40
50
60
70
80
90
17
Yss
22
20
Ysa
18
— Yss array
--- Ysa array

Fig 3.


100
90
80
70
60
50
40
30
40
50
60
70
80
90
A
B
C
17
Yss
Ysa
18
— Yss array
--- Ysa array

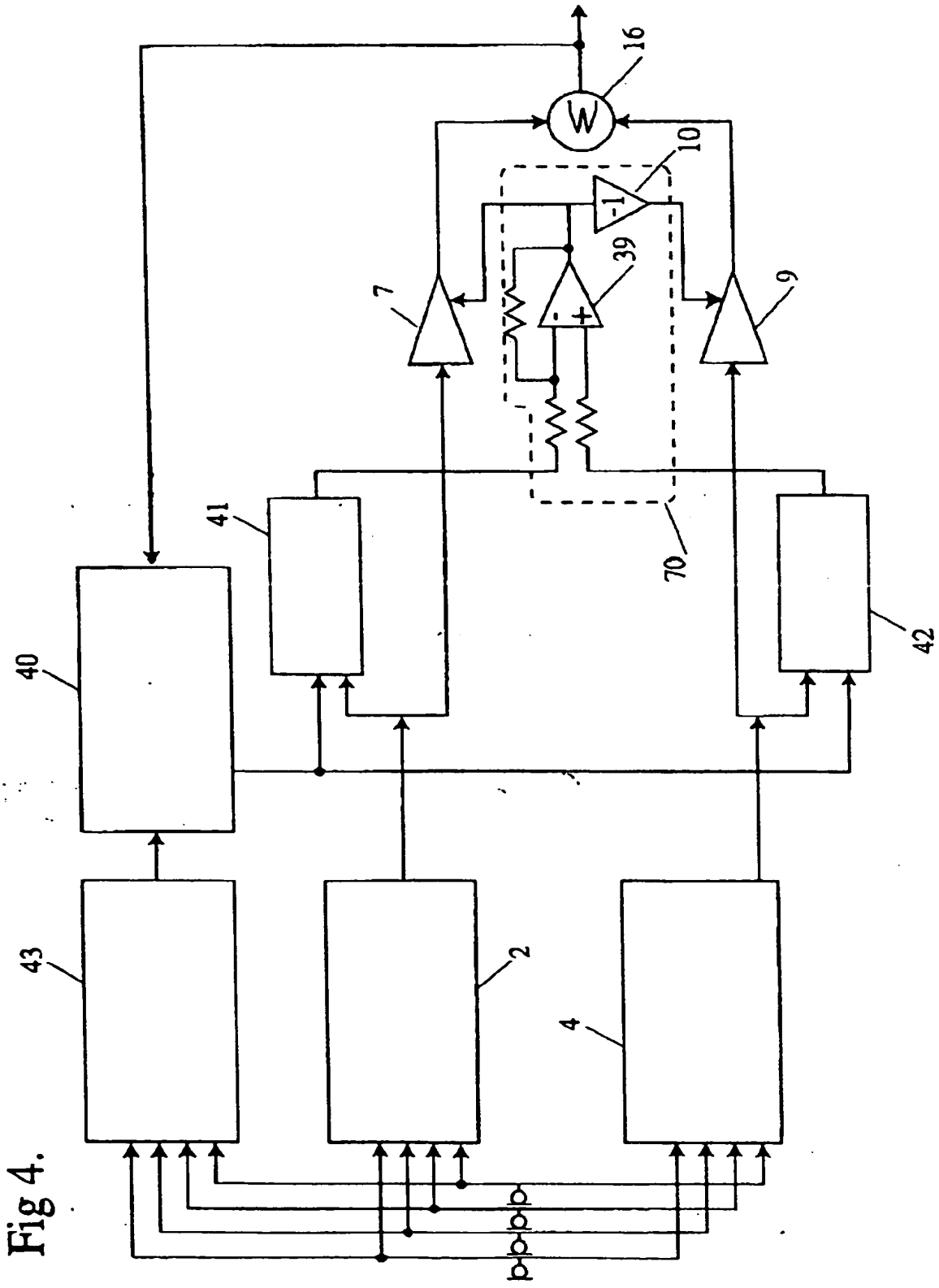


Fig 4.

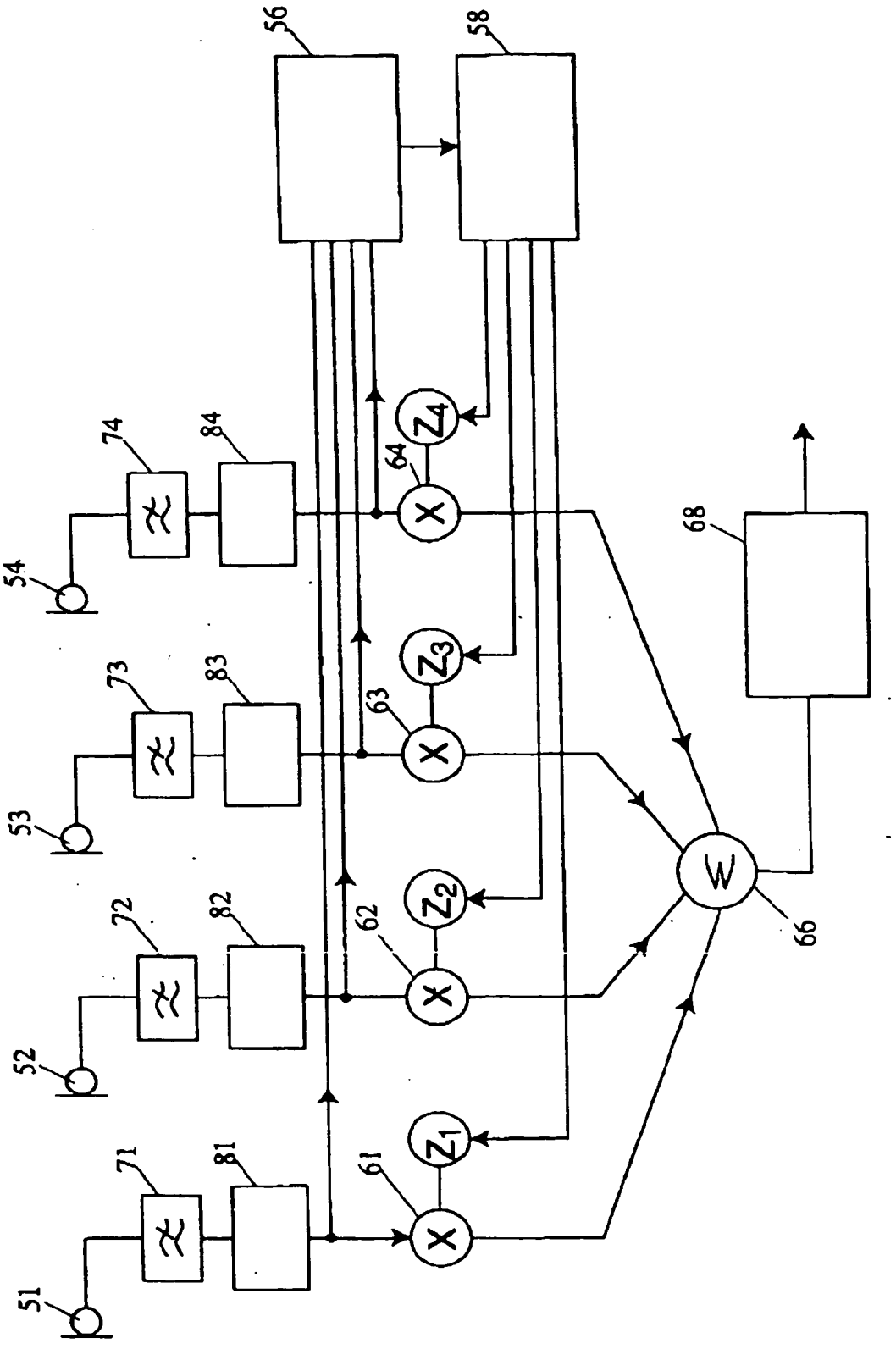


Fig 5.

THIS PAGE BLANK (USPTO)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 883 325 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
27.12.2000 Bulletin 2000/52

(43) Date of publication A2:
09.12.1998 Bulletin 1998/50

(21) Application number: **98304349.8**

(22) Date of filing: **02.06.1998**

(51) Int Cl.[7]: **H04R 3/00**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **02.06.1997 AU PO714197**

(71) Applicant: **THE UNIVERSITY OF MELBOURNE**
Parkville, Victoria 3052 (AU)

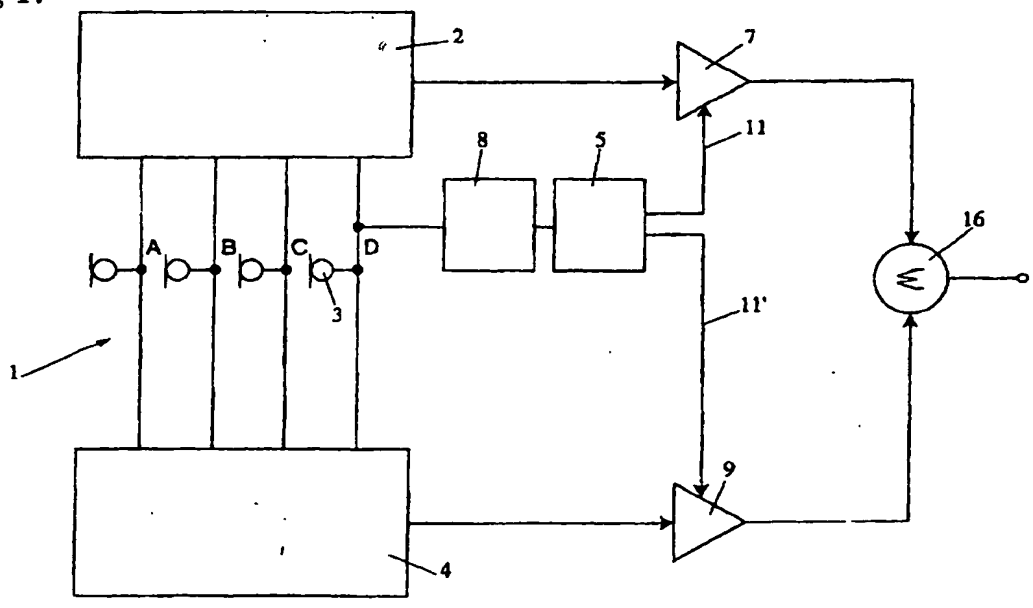
(72) Inventors:
- **Raicevich, George**
  Stanmore, N.S.W. 2204 (AU)
- **Dillon, Harvey**
  Turramurra, N.S.W. 2074 (AU)

(74) Representative: **Molyneaux, Martyn William**
Langner Parry
52-54 High Holborn
London WC1V 6RR (GB)

(54) Multi-strategy array processor

(57) An apparatus and method for processing sound, suitable for use in association with a hearing aid, cochlear implant prosthesis or the like. Coupled to an array of microphones (1) are a pair of fixed array processors (2,4) each having different characteristic signal-to-noise performances and internal noise parameters in different levels of ambient noise. Based upon an ambient noise estimate derived from noise floor detector (8) a control circuit (5) controls the gain of a pair of VCA's (7,9) coupled to the fixed array processors (2,4) in order to produce an output signal from summer (16) which maximises the signal-tonoise ratio of a signal emanating from a source in an on-beam direction relative to the microphone array (10).

Fig 1.



EP 0 883 325 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 4349

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 5 574 824 A (SLYH RAYMOND E ET AL) 12 November 1996 (1996-11-12) * column 2, line 44-63 * * column 5, line 22 - column 7, line 29 *	1,2,5-7, 9,12,13, 19-21, 23,24	H04R3/00
A	* column 8, line 44 - column 9, line 24 * * column 11, line 52 - column 16, line 20 *	3,4,10, 11,14, 15,17,18	
Y	WO 96 13096 A (COCHLEAR PTY LTD ;SELIGMAN PETER (AU)) 2 May 1996 (1996-05-02) * page 1, line 3-5 * * page 2, line 23-32 *	1,2,5-7, 9,12,13, 19-21, 23,24	
A	* page 3, line 18 - page 4, line 16 *	10	
A	GB 2 306 086 A (TRIM RICHARD MORRIS ;DOCKLANDS LIGHT RAILWAY LIMITE (GB)) 23 April 1997 (1997-04-23) * page 1, line 1-3 * * page 2, line 9 - page 3, line 3 * * page 3, line 7 - page 5, line 7 *	10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04R G01S H03G G10L
A	WO 95 34983 A (VOLVO AB ;NORDEBO SVEN (SE); NORDHOLM SVEN (SE); CLAESSON INGVAR () 21 December 1995 (1995-12-21) * page 4, line 28-35 * * page 5, line 26 - page 8, line 18 *	14	
A	US 5 548 681 A (GLEAVES DAVID ET AL) 20 August 1996 (1996-08-20) * column 4, line 39-50 * * figure 1 * -/--	14,16, 19,22	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 November 2000	Zanti, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 4349

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 931 977 A (KLEMES MAREK) 5 June 1990 (1990-06-05) * column 1, line 13-20 * * column 6, line 12-21 * * column 6, line 35 - column 7, line 18 *	14	
A	US 4 802 227 A (ELKO GARY W ET AL) 31 January 1989 (1989-01-31) * column 2, line 35 - column 3, line 21 * * column 4, line 18 - column 11, line 60 *	1-24	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 November 2000	Zanti, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 98 30 4349

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

07-11-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5574824 A	12-11-1996	NONE	
WO 9613096 A	02-05-1996	AU 689659 B	02-04-1998
		AU 3737695 A	15-05-1996
		CA 2203395 A	02-05-1996
		EP 0787383 A	06-08-1997
		JP 10507603 T	21-07-1998
GB 2306086 A	23-04-1997	NONE	
WO 9534983 A	21-12-1995	SE 502888 C	12-02-1996
		AU 2759495 A	05-01-1996
		EP 0765562 A	02-04-1997
		JP 10501668 T	10-02-1998
		SE 9402088 A	15-12-1995
US 5548681 A	20-08-1996	JP 5323993 A	07-12-1993
US 4931977 A	05-06-1990	NONE	
US 4802227 A	31-01-1989	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82